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10/820,500	04/07/2004	Ping-Ying Wang	251806-1060	7397

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
TIMORY, KABIR A	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
10/18/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.	Applicant(s)	
	10/820,500	WANG, PING-YING	
	Examiner	Art Unit	
	Kabir A. Timory	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a spread spectrum control circuit as recited in claims 17, 19, 25, 28, 32, 35 and a frequency control circuit as recited in claims 17, 19, 28, 32, and 35 respectively must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next

Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

2. Applicant's arguments with respect to claims 17-39 have been considered but are moot in view of new ground(s) of rejection because of the amendment.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 17-21, 25-28, and 32-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyabe et al. (US Patent Number 6,559,698).

Regarding claims 17, 25, and 32:

As shown in figures 1, Miyabe et al. discloses a clock generating circuit, comprising:

- a clock generator (1 in figure 1) for receiving a reference clock signal (4 in figure 1) and thereby generating an output clock signal (14 in figure 1); and
- a spread spectrum control circuit (clock modulation circuit is interpreted to be the spread spectrum control circuit) (2 in figure 1), coupled to the clock generator (1 in figure 1), for generating a modulated clock signal with frequency variation (19, a in figure 1) according to the output clock signal and a modulation value (column 5, lines 16-32), comprising:
- a modulation value generating circuit (19 in figure 1) for outputting the modulation value (a in figure 1); and
- a frequency control circuit (15 in figure 1), coupled to the clock generator (1 in figure 1) and the modulation value generating circuit (19 in figure 1), for generating the modulated clock signal according to the output clock signal (14 in figure 1) and the modulation value (19, a in figure 1) with which an average frequency of the modulated clock signal varies (column 5, lines 57-67, and column 6, lines 1-29);
- wherein the clock generator operates in a way being independent of the spread spectrum control circuit, and the modulation value varies with time in a predetermined manner so as to force the average frequency of the modulated clock signal to change up and down over time (column 5, lines 57-67, and column 6, lines 1-29).

Regarding claims 18 and 26:

Miyabe et al. further discloses wherein the predetermined manner represents that the modulation value increases progressively in a first period of time and then

decreases progressively in a second period of time so as to force the average frequency of the modulated clock signal to change over time (figure 2).

Regarding claims 19 and 27:

Miyabe et al. further discloses wherein the modulation value generating circuit (19 in figure 1) outputs the modulation value (19, a in figure 1) according to at least one of an external control and the average frequency of the modulated clock signal (18 in figure 1, column 5, lines 16-67, and column 6, lines 1-29).

Regarding claims 20, 28, and 35:

Miyabe et al. further discloses wherein the spread spectrum control circuit further comprises: a timing control circuit (17 in figure 1), coupled between the modulation value generating (19 in figure 1) circuit and the frequency control circuit (15 in figure 1), for providing a frequency control value for the frequency control circuit according the modulation value after a predetermined period of time such that the average frequency of the modulated clock signal changes in accordance with the frequency control value after the predetermined period of time (column 5, lines 16-67, and column 6, lines 1-29).

Regarding claim 21:

Miyabe et al. further discloses wherein the timing control circuit is a delta-sigma modulator (21 in figure 1).

Regarding claim 33:

Miyabe et al. further discloses wherein the clock generator operates in a way being independent of the spread spectrum control circuit (1 in figure 1).

Regarding claim 34:

Miyabe et al. further discloses wherein the modulation value generating circuit (19 in figure 1) outputs the control values according to at least one of an external control and the average frequency of the modulated clock signal (19 a in figure 1, (column 5, lines 16-67, and column 6, lines 1-29).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 22-24, 29-31, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyabe et al. (US Patent Number 6,559,698) as applied to claims17, 25 and 32 in view of Pitzer et al. (US Patent Number 6,876,710) and further in view of Kim et al. (US Pub. Number 2004/0001600).

Regarding claims 22, 29, and 36:

Miyabe et al. discloses all of the subject matter as described above except for specifically teaching wherein the clock generator is a multi-phase clock generator for generating the output clock signal including a plurality of oscillation clock signals having a same frequency but different phases.

However, Pitzer et al. in the same field of endeavor, teaches wherein the clock generator is a multi-phase clock generator for generating the output clock signal (12 in figure 1).

Miyabe et al. and Pitzer et al. disclose all of the subject matter as described above except for specifically teaching including a plurality of oscillation clock signals having a same frequency but different phases.

However, Kim et al. in the same field of endeavor, teaches including a plurality of oscillation clock signals having a same frequency but different phases (clock signal having the same period is interpreted to be the signals having the same frequency) (figure 3 and figure 5A-5F, paragraph 0025, lines 1-5).

One of ordinary skill in the art would have clearly recognized that in spread spectrum clock generating and multiphase clock generating system a multiphase clock generator is used to generate multiple clock signal for the system as taught by Pitzer et al. in digitally controlled circuit for reducing the phase modulation of a signal. In order to avoid signal overlapping, the generated clock signals, which have the same periods or frequencies, should be different or shifted in phase. Therefore, in order to overcome the overlapping, it would have been obvious to one ordinary skill in the art at the time the invention was made to shift the phase of signal as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. Multiple generated clock signal which have the same frequency but different phases in advantageous because by shifting the phase of generated clock signal we can avoid signal overlapping in the system.

Regarding claims 23, 30, and 37:

Miyabe et al. further discloses the modulation value generating circuit and outputting one of them as the modulated clock signal according to the modulation value (19, a in figure 1).

Miyabe et al. and Pitzer et al. disclose all of the subject matter as described above except for specifically teaching wherein the frequency control circuit comprises:

- a phase interpolator, coupled to the clock generator, for generating a plurality of interpolation signals according to at least two of the oscillation clock signals; and
- a phase selector, coupled to the phase interpolator and the modulation value generating circuit, for receiving the plurality of interpolation signals and outputting one of them as the modulated clock signal according to the modulation value.

However, Kim et al. in the same field of endeavor, teaches wherein the frequency control circuit comprises:

- a phase interpolator (18 in figure 1), coupled to the clock generator (24 in figure 1), for generating a plurality of interpolation signals according to at least two of the oscillation clock signals (CLK0-CLK(n-1)); and
- a phase selector (20 in figure 1), coupled to the phase interpolator (18 in figure 1) and, for receiving the plurality of interpolation signals (paragraph 0031, lines 6-7).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system and spread spectrum clock generating system in order to select clock signals among plurality of clock signals, a clock or phase selector is required. Also to generate phase-shifted signals, an interpolator is used in the system.

Interpolator receives the clock signal and generates first through n-th discrete clock signals having the same period but shifted in phase by predetermined offsets so as to not to overlap one another. In order to select and generate phase-shifted signals, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a phase selector and an interpolator as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including phase selector and interpolator, we can generate phase-shifted signals and select the desired clock signals in the system.

Regarding claims 24, 31, and 38:

Miyabe et al. and Pitzer et al. disclose all of the subject matter as described above except for specifically teaching wherein the frequency control circuit comprises: a phase selector, coupled to the clock generator, for outputting at least two of the oscillation clock signals as selection signals; and a phase interpolator, coupled to the phase selector, for generating the modulated clock signal according to the selection signals; wherein at least one of the phase selector and the phase interpolator operates according to the modulation value.

However, Kim et al. in the same field of endeavor, teaches teaching wherein the frequency control circuit comprises:

- a phase selector (20 in figure 1), coupled to the clock generator (24 in figure 1), for outputting at least two of the oscillation clock signals as selection signals (figure 3); and

- a phase interpolator (18 in figure 1), coupled to the phase selector (20 in figure 1), for generating the modulated clock signal according to the selection signals (CLK0-CLK(n-1));
- wherein at least one of the phase selector and the phase interpolator operates according to the modulation value (figure 6, paragraph 0031, lines 6-7).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system and spread spectrum clock generating system in order to select clock signals among plurality of clock signals, a clock or phase selector is required. Also to generate phase-shifted signals, an interpolator is used in the system. Interpolator receives the clock signal and generates first through n-th discrete clock signals having the same period but shifted in phase by predetermined offsets so as to not to overlap one another. In order to select and generate phase-shifted signals, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a phase selector and an interpolator as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including phase selector and interpolator, we can generate phase-shifted signals and select the desired clock signals in the system.

7. Claim 39 is ejected under 35 U.S.C. 103(a) as being unpatentable over Miyabe et al. (US Patent Number 6,559,698) in view of Kim et al. (US Pub. Number 2004/0001600).

Regarding claim 39:

Miyabe et al. discloses all of the subject matter as described above except for specifically teaching wherein the medium values are different.

However, Kim et al. in the same field of endeavor, teaches wherein the medium values are different (clock signal having the same period is interpreted to be medium values are different) (figure 3 and figure 5A-5F, paragraph 0025, lines 1-5).

One of ordinary skill in the art would have clearly recognized that in spread spectrum clock generating and multiphase clock generating system a multiphase clock generator is used to generate multiple clock signal for the system as taught by Pitzer et al. in digitally controlled circuit for reducing the phase modulation of a signal. In order to avoid signal overlapping, the generated clock signals, which have the same periods or frequencies, should be different or shifted in phase. Therefore, in order to overcome the overlapping, it would have been obvious to one ordinary skill in the art at the time the invention was made to shift the phase of signal as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. Multiple generated clock signal which have the same frequency but different phases in advantageous because by shifting the phase of generated clock signal we can avoid signal overlapping in the system.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kabir A. Timory whose telephone number is 571-270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kabir A. Timory
October 5, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER